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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,690	10/14/2003	Xiaohua Shi	INTEL/17586	3406

7590 06/28/2006

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EXAMINER	
INGBERG, TODD D	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/684,690	SHI ET AL.	
	Examiner	Art Unit	
	Todd Ingberg	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 25 have been examined.

Information Disclosure Statement

1. The Information Disclosure Statement filed November 17, 2003 has been considered.

Drawings

2. The drawings filed November 17, 2003 have been accepted.

Specification

3. The abstract of the disclosure is objected to because legal words such as "method", "apparatus" etc present. Correction is required. See MPEP § 608.01(b).

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Legal words should be removed.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1 - 25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The current focus of the Patent Office in regard to statutory inventions under 35 U.S.C. § 101 for method claims and claims that recite a judicial exception (software) is that the claimed invention recite a practical application. Practical application can be provided by a physical transformation or a useful, concrete and tangible result. No physical transformation is recited and additionally, the final result of the claim is escape analysis which is not a tangible result because the end result of the escape analysis is not claimed to be tangibly

embodied on a compute readable medium. The following link on the World Wide Web is for the United States Patent And Trademark Office (USPTO) policy on 35 U.S.C. §101.

<http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf>

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1 – 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Compositional Pointer and Escape Analysis for Java Programs, John Whaley et al, 1999, ACM (ESC) in view of "Effective Synchronization Removal for Java", Erik Ruf, ACM, 2000 (IDS).

Claim 1
ESC teaches a method to analyze escape analysis of an application comprising: identifying one or more methods associated with a violating condition (ESC, page 192, section 3.3); parsing the one or more methods into at least one equivalence class (IDS, page 209 section 2.2 - the Directed Acyclic Graphs are proof of parsing they are the result and required for section 3.3.2); identifying a first escape indicator and a second escape indicator associated with each of the at least one equivalence class (IDS, as per above); and propagating the one or more methods based on the first and second escape indicators (ESC, as per above). ESC teaches escape pointer analysis for JAVA, where the program prepares for an early exit. What ESC does not explicitly mention is the well known transformation for optimization known as equivalence. It is IDS who teaches the well known optimization technique in the context of Java. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to combine ESC and IDS because equivalence optimization is a low level optimization technique and will result in making programs that prepare for the encountering of an escape more efficient.

Claim 2
A method as defined in claim 1, wherein identifying the one or more methods associated with the violating condition comprises identifying at least one of a new method, an additional method, and a method associated with a change in a recursive call chain (ESC, page 190, section 2.3).

Claim 3
A method as defined in claim 1, wherein identifying the one or more methods associated with the violating condition comprises identifying one or more methods associated with at least one of dynamic class loading, native method, and reflection (ESC, page 202, Dynamic classloading result of classes produced by Jalapeno).

Claim 4
A method as defined in claim 1, wherein identifying the one or more methods associated with the violating condition comprises identifying the one or more methods during runtime of the application.(ESC, page 192, section 3.3).

Claim 5
A method as defined in claim 1, wherein identifying the first escape indicator and the second escape indicator associated with each of the at least one class comprises identifying a bottom-up escape status flag and a top-down escape status flag. (ESC, page 18, section 1.3, required for edges of the graph – how to plan to escape from a segment (basic block) of code).

Claim 6
A method as defined in claim 1, further comprising updating the escape analysis of the application. (Inherent – while the program runs the program lookup table is the possible paths traversing the DAG and the conditions of the code control the actual course of the program. Escapes interrupt that course and must be updated same as the current course of the program).

Claim 7
A machine readable medium storing instructions, which when executed, cause a machine to: identify one or more methods associated with a violating condition; parse the one or more methods into at least one equivalence class; identify a first escape indicator and a second escape indicator associated with each of the at least one class; and propagate the one or more methods based on the first and second escape indicators. As per claim 1.

Claim 8
A machine readable medium as defined in claim 7, wherein the instructions cause the machine to identify the one or more methods associated with the violating condition by identifying at least one of a new method, an additional method, and a method associated with a change in a recursive call chain. As per claim 2.

Claim 9
A machine readable medium as defined in claim 7, wherein the instructions cause the machine to identify the one or more methods associated with the violating condition by identifying one or more methods associated with at least one of dynamic class loading, native method, and reflection. As per claim 3.

Claim 10
A machine readable medium as defined in claim 7, wherein the instructions cause the machine to identify the one or more methods associated with the violating condition by identifying the one or more methods during runtime of the application. As per claim 4.

Claim 11
A machine readable medium as defined in claim 7, wherein the instructions cause the machine identify the first escape indicator and the second escape indicator associated with each of the at least one class by identifying a bottom-up escape status flag and a top-down escape status flag. As per claim 5.

Claim 12
A machine readable medium as defined in claim 7, further comprising instructions, which when executed, cause the machine to update the escape analysis of the application. As per claim 6.

Claim 13
A machine readable medium as defined in claim 7, wherein the machine readable medium comprises one of a programmable gate array, an application specific integrated circuit, an erasable programmable read only memory, a read only memory, random access memory, a magnetic media, and an optical media. (JAVA running in the RAM environment required for the techniques disclosed in both ESC and IDS).

Claim 14
An apparatus to analyze escape analysis of an application comprising: a method identifier configured to identify one or more methods associated with a violating condition; a method parser coupled to the method identifier and configured to parse the one or more methods into at least one class; a status identifier coupled to the method parser and configured to identify a first status indicator and a second status indicator associated with the least one class; and a compiler coupled to the status identifier and configured to propagate the one or more methods based on the first and second status indicators. As per claim 1.

Claim 15
An apparatus as defined in claim 14, wherein one or more methods associated with a violating condition comprises at least one of a new method, an additional method, and a method associated with a change in a recursive call chain. As per claim 2.

Claim 16
An apparatus as defined in claim 14, wherein the violating condition comprises at least one of dynamic class loading, native method, and reflection. As per claim 3.

Claim 17
An apparatus as defined in claim 14, wherein the first escape indicator comprises a bottom-up escape status flag. As per claim 4.

Claim 18
An apparatus as defined in claim 14, wherein the second escape indicator comprises a top-down escape status flag. As per claim 5.

Claim 19
An apparatus as defined in claim 14, wherein the compiler is configured to update the escape analysis of the application. As per claim 6.

Claim 20
A processor system to analyze escape analysis of an application comprising: a dynamic random access memory (DRAM) configured to store one or more methods of the application;
a processor operatively coupled to the DRAM, the processor being programmed to identify the one or more methods associated with the violating condition, to parse the one or more methods into at least one equivalence class, to identify a first escape indicator and a second escape indicator associated with each of the at least one class, and to propagate the one or more methods based on the first and second escape indicators. As per claim 1.

Claim 21
A processor system as defined in claim 20, wherein the one or more methods associated with a violating condition comprises at least one of a new method, an additional method, and a method associated with a change in a recursive call chain. As per claim 2.

Claim 22
A processor system as defined in claim 20, wherein the violating condition comprises at least one of dynamic class loading, native method, and reflection. As per claim 3.

Claim 23
A processor system as defined in claim 20, wherein the first escape indicator comprises a bottom-up escape status flag. As per claim 4.

Claim 24
A processor system as defined in claim 20, wherein the second escape indicator comprises a top-down escape status flag. As per claim 5.

Claim 25
A processor system as defined in claim 20, wherein the processor is configured to update the escape analysis of the application. As per claim 6.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Todd Ingberg whose telephone number is (571) 272-3723. The examiner can normally be reached on during the work week..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Todd Ingberg
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Art Unit 2193

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